AMENDMENTS TO THE CLAIMS

Claims 2-12, 14-24, 26-33, 35-42, and 44-49 remain as previously pending. Please amend Claims 1, 13, 25, 34, and 43 as indicated below.

1. (Currently Amended) A semiconductor structure comprising:

a polysilicon layer;

a barrier layer above the polysilicon layer, the barrier layer comprising tungsten silicide having tungsten-rich areas, the tungsten-rich areas forming tungsten oxynitride in the presence of oxygen and nitrogen, wherein the tungsten oxynitride expands relative to the barrier layer to extend outwardly from the sides of the barrier layer to form tungsten oxynitride extrusions, wherein the barrier layer has substantially etched tungsten oxynitride extrusions formed on the side thereof;

a conductive layer above the barrier layer, the conductive layer comprising titanium silicide having titanium-rich areas, the titanium-rich areas forming titanium oxynitride in the presence of oxygen and nitrogen, wherein the titanium oxynitride expands relative to the conductive layer to extend outwardly from the sides of the conductive layer to form titanium oxynitride extrusions, wherein the conductive layer has substantially etched titanium oxynitride extrusions formed on the side thereof; and

a cap above the conductive layer.

2. (Original) The semiconductor structure of Claim 1 wherein the semiconductor structure comprises at least a portion of a transistor.

3. (Original) The semiconductor structure of Claim 1 wherein the semiconductor structure comprises at least a portion of a synchronous dynamic random access memory array.

4. (Original) The semiconductor structure of Claim 1 wherein the semiconductor structure comprises at least a portion of a static memory array.

5. (Original) The semiconductor structure of Claim 1 wherein the semiconductor structure comprises at least a portion of a dynamic memory array.

6. (Original) The semiconductor structure of Claim 1 wherein the semiconductor structure comprises at least a portion of an extended data out memory array.

7. (Original) The semiconductor structure of Claim 1 wherein the semiconductor structure comprises at least a portion of a wordline in a memory array.

8. (Original) The semiconductor structure of Claim 1 wherein the barrier layer is approximately 150 Å thick.

9. (Original) The semiconductor structure of Claim 1 wherein the barrier layer has a resistivity of approximately 60 μΩ-cm.

10. (Original) The semiconductor structure of Claim 1 wherein the conductive layer is approximately 1000 Å thick.

11. (Original) The semiconductor structure of Claim 1 wherein the conductive layer has a resistivity of approximately 15-20 μΩ-cm.

12. (Original) The semiconductor structure of Claim 1 wherein the polysilicon layer is above a semiconductor substrate comprising silicon.

13. (Currently Amended) A semiconductor structure comprising:

a polysilicon layer;

a barrier layer above the polysilicon layer, the barrier layer comprising metal silicide having metal-rich areas, the metal-rich areas forming metal oxynitride in the presence of oxygen and nitrogen, wherein the metal oxynitride expands relative to the barrier layer to extend outwardly from the sides of the barrier layer to form metal oxynitride extrusions, wherein the barrier layer has substantially etched metal oxynitride extrusions formed on the side thereof;

a conductive layer above the barrier layer, the conductive layer comprising metal silicide having metal-rich areas, the metal-rich areas forming metal oxynitride in the presence of oxygen and nitrogen, wherein the metal oxynitride expands relative to the conductive layer to extend outwardly from the sides of the conductive layer to form metal oxynitride extrusions, wherein the conductive layer has substantially etched metal oxynitride extrusions formed on the side thereof; and

a cap above the conductive layer.

14. (Original) The semiconductor structure of Claim 13 wherein the semiconductor structure comprises at least a portion of a transistor.

15. (Original) The semiconductor structure of Claim 13 wherein the semiconductor structure comprises at least a portion of a synchronous dynamic random access memory array.

16. (Original) The semiconductor structure of Claim 13 wherein the semiconductor structure comprises at least a portion of a static memory array.

17. (Original) The semiconductor structure of Claim 13 wherein the semiconductor structure comprises at least a portion of a dynamic memory array.

18. (Original) The semiconductor structure of Claim 13 wherein the semiconductor structure comprises at least a portion of an extended data out memory array.

19. (Original) The semiconductor structure of Claim 13 wherein the semiconductor structure comprises at least a portion of a wordline in a memory array.

20. (Original) The semiconductor structure of Claim 13 wherein the barrier layer is approximately 150 Å thick.

21. (Original) The semiconductor structure of Claim 13 wherein the barrier layer has a resistivity of approximately 60 μΩ-cm.

22. (Original) The semiconductor structure of Claim 13 wherein the conductive layer is approximately 1000 Å thick.

23. (Original) The semiconductor structure of Claim 13 wherein the conductive layer has a resistivity of approximately 15-20 μΩ-cm.

24. (Original) The semiconductor structure of Claim 13 wherein the polysilicon layer is above a semiconductor substrate comprising silicon.

25. (Currently Amended) A semiconductor stack in a semiconductor device having at least a side comprising a tungsten silicide layer having tungsten-rich areas, the tungsten-rich areas forming tungsten oxynitride in the presence of oxygen and nitrogen, wherein the tungsten oxynitride expands relative to the tungsten silicide layer to extend outwardly from the side of the tungsten silicide layer to form tungsten oxynitride extrusions, wherein the tungsten silicide layer has substantially etched tungsten oxynitride extrusions formed on the side thereof.

26. (Original) The semiconductor stack of Claim 25, wherein the semiconductor stack comprises at least a portion of a transistor.

27. (Original) The semiconductor stack of Claim 25, wherein the semiconductor stack comprises at least a portion of a synchronous dynamic access random memory array.

28. (Original) The semiconductor stack of Claim 25, wherein the semiconductor stack comprises at least a portion of a static memory array.

29. (Original) The semiconductor stack of Claim 25, wherein the semiconductor stack comprises at least a portion of a dynamic memory array.

30. (Original) The semiconductor stack of Claim 25, wherein the semiconductor stack comprises at least a portion of an extended data out memory array.

31. (Original) The semiconductor stack of Claim 25, wherein the semiconductor stack comprises at least a portion of a wordline in a memory array.

32. (Original) The semiconductor stack of Claim 25, wherein the tungsten silicide layer is approximately 150 Å thick.

33. (Original) The semiconductor stack of Claim 25, wherein the tungsten silicide layer has a resistivity of approximately 60 μΩ-cm.

34. (Currently Amended) A semiconductor stack in a semiconductor device having at least a side comprising a titanium silicide layer having titanium-rich areas, the titanium-rich areas forming titanium oxynitride in the presence of oxygen and nitrogen, wherein the titanium oxynitride expands relative to the titanium silicide layer to extend outwardly from the side of the titanium silicide layer to form titanium oxynitride extrusions, wherein the titanium silicide layer has substantially etched titanium oxynitride extrusions formed on the side thereof.

35. (Original) The semiconductor stack of Claim 34, wherein the semiconductor stack comprises at least a portion of a transistor.

36. (Original) The semiconductor stack of Claim 34, wherein the semiconductor stack comprises at least a portion of a synchronous dynamic access random memory array.

37. (Original) The semiconductor stack of Claim 34, wherein the semiconductor stack comprises at least a portion of a static memory array.

38. (Original) The semiconductor stack of Claim 34, wherein the semiconductor stack comprises at least a portion of a dynamic memory array.

39. (Original) The semiconductor stack of Claim 34, wherein the semiconductor stack comprises at least a portion of an extended data out memory array.

40. (Original) The semiconductor stack of Claim 34, wherein the semiconductor stack comprises at least a portion of a wordline in a memory array.

41. (Original) The semiconductor stack of Claim 34, wherein the titanium silicide layer is approximately 1000 Å thick.

42. (Original) The semiconductor stack of Claim 34, wherein the titanium silicide layer has a resistivity of approximately 15-20 μΩ-cm.

43. (Currently Amended) A semiconductor stack having at least a side comprising a metal silicide layer having metal-rich areas, the metal-rich areas forming metal oxynitride in the presence of oxygen and nitrogen, wherein the metal oxynitride expands relative to the metal silicide layer to extend outwardly from the side of the metal silicide layer to form metal oxynitride extrusions, wherein the metal silicide layer has substantially etched metal oxynitride extrusions formed on the side thereof.

44. (Original) The semiconductor stack of Claim 43, wherein the semiconductor stack comprises at least a portion of a transistor.

45. (Original) The semiconductor stack of Claim 43, wherein the semiconductor stack comprises at least a portion of a synchronous dynamic access random memory array.

46. (Original) The semiconductor stack of Claim 43, wherein the semiconductor stack comprises at least a portion of a static memory array.

47. (Original) The semiconductor stack of Claim 43, wherein the semiconductor stack comprises at least a portion of a dynamic memory array.

48. (Original) The semiconductor stack of Claim 43, wherein the semiconductor stack comprises at least a portion of an extended data out memory array.

49. (Original) The semiconductor stack of Claim 43, wherein the semiconductor stack comprises at least a portion of a wordline in a memory array.